[0075] In one embodiment, an additional resistor—a third resistor **523***c*—is coupled between node **527** and the first and second resistor-switches. In one embodiment, the value of the resistors ranges from a few 1 KOhms to approximately 10 kOhms.

[0076] FIG. **6** is a schematic of a switch-resistor core **600**, according to one embodiment of the invention. FIG. **6** is a version of FIG. **5**B without resistor **523***c*. FIG. **6** is the functional equivalent of FIG. **5**B assuming a break-before-make operation of the switches in FIG. **5**B.

[0077] The switch-resistor core **600** comprises a multiplexer-like circuit topology with VH and VL being inputs which are selectable by control signals C and C#, which correspond to signal **107** (e.g., C**1**, C**1**#), and VxTri signal being the output signal (e.g., Vx,**0**; Vx,**1** of FIGS. **5**A-C). The transistors discussed herein are referred with labels "first," "second," third," etc for ease of describing the embodiments.

[0078] In one embodiment, the select control signal C is received as input to the gate terminals of a first PMOS transistor MPS**1** and a first NMOS transistor MNS**1**. The source/drain terminal of MPS**1** receives signal VL while its other drain/source terminal is coupled to a drain/source terminal of a second PMOS transistor MPS**2** and to the output node carrying VxTri signal. The source/drain terminal of the first NMOS transistor MNS**1** receives signal VH while its other drain/source terminal is coupled to a drain/source terminal of the second NMOS transistor MNS**2** and to the output node carrying the VxTri signal.

[0079] In one embodiment, the select control signal C#, which is complementary signal of C, is received as input to the gate terminals of the second PMOS transistor MPS**2** and the second NMOS transistor MNS**2**. The source/drain terminal of the second PMOS transistor MPS**2** receives signal VH while its other drain/source terminal is coupled to a drain/source terminal of the first PMOS transistor MPS**1** and to the output node carrying the VxTri signal. The source/drain terminal of the second PMOS transistor MNS**2** receives signal VL while its other drain/source terminal is coupled to a drain/source terminal of the first NMOS transistor MNS**1** and to the output node carrying the VxTri signal.

[0080] While the embodiment of FIG. **6** illustrates single transistors, they can be replaced with transmission gates having PMOS and NMOS transistors coupled in parallel to another. For example, the NMOS transistors coupled to VH can be pass gates while the PMOS transistor receiving VL can continue to be regular single transistor pass gates. Any combination of pass-gates and single transistor pass gates may be used and corresponding control signals may be re-wired to realize the same truth table of the embodiment of FIG. **6**.

[0081] FIG. **7** is a schematic of a switch-resistor cell **700** having the switch-resistor core **701**, according to one embodiment of the invention. In one embodiment, the switch-resistor cell **700** comprises the switch-resistor core **701**. The switch-resistor core **701** comprises NMOS transistors MN**1**-MN**4** and PMOS transistors MP**1**-MP**4** which are operable to be selected by control signals C and C# to pass VH or VL as the VxTri signal. The switch-resistor core **701** is similar to the switch-resistor **600** of FIG. **6**. In one embodiment, the transistors MN**7** and MN**9** are always ON to control the resistance of the RC filter formed by the switch-resistor cell **701**.

[0082] In one embodiment, the switch-resistor cell **701** is operable to be disabled when the phase of the switch-resistor cell is not being used. In such an embodiment, the VxTri signal is tri-stated. The disabling and enabling of the switch-resistor cell **701** is performed by transistors in blocks **702** and **704**. This capability in the switch-resistor cell **701** allows for selectively enabling or disabling of the switch-resistor cells in the switch-resistor array **102** to reduce power consumption when needed. For example, when a phase generated by the switch-resistor cell is not being used, the switch-resistor cell associated with that phase can be disabled.

[0083] In one embodiment, blocks **702** and **704** comprise NMOS transistors MN**8** and MN**10** to block the passing of VH and VL as the VxTri signal via the switch-resistor cell **701**. In one embodiment, the passing of VH and VL is blocked by disabling the NMOS transistors MN**8** and MN**10** via signal NE. In this embodiment, blocks **702** and **704** also comprise PMOS transistors MP**7** and MP**9** to block the passing of VH and VL as VxTri via the switch-resistor cell **701** by disabling the PMOS transistors MP**7** and MP**9** via signal PE. The signal PE is complementary to the signal NE. In one embodiment transistors MN**7**, MN**9**, MP**8**, and MP**10** are always turned on to control the resistance in the RC filter of the switch-resistor cell **701**. In one embodiment, signals NE and PE are generated by the circuit discussed with reference to FIG. **9**. In one embodiment, transistor MP**8** is positioned between transistors MP**2** and MP**4** such that transistor MP**2** couples to transistor MP**6** via their respective source/drain terminals. By positioning transistor MP**8** between transistors MP**2** and MP**4**, additional RC filtering is achieved by the switch-resistor cell **701** resulting in smoother VxTri signal. In one embodiment, transistor MP**10** is positioned between transistors MP**2** and MP**4** such that transistor MP**4** couples to transistor MP**12** via their respective source/drain terminals. By positioning transistor MP**12** between transistors MP**2** and MP**4** additional RC filtering is achieved by the switch-resistor cell **701** resulting in smoother VxTri signal.

[0084] In one embodiment, transistor MN**7** is positioned between transistors MN**1** and MN**2** such that transistor MN**1** couples to transistor MN**5** via their respective source/drain terminals. By positioning transistor MN**7** between transistors MN**1** and MN**2** additional RC filtering is achieved by the switch-resistor cell **701** resulting in smoother VxTri signal. In one embodiment, transistor MN**9** is positioned between transistors MN**1** and MN**2** such that transistor MN**1** couples to transistor MN**9** via their respective source/drain terminals. By positioning transistor MN**9** between transistors MN**1** and MN**2** additional RC filtering is achieved by the switch-resistor cell **701** resulting in smoother VxTri signal.

[0085] In one embodiment, the switch-resistor core **700** further comprises blocks **703** and **705** having transistors which are controllable by signals P and PB. Signal PB is complementary of signal P. The transistors controlled by the signal P include NMOS transistors MN**5** and MN**6**, and PMOS transistors MP**11** and MP**12**. The transistors controlled by the signal PB include NMOS transistors MN**11** and MN**12**, and PMOS transistors MP**5** and MP**6**. In this embodiment, signals P and PB are used for adjusting phase angle of the phase generated by the switch-resistor cell **701**